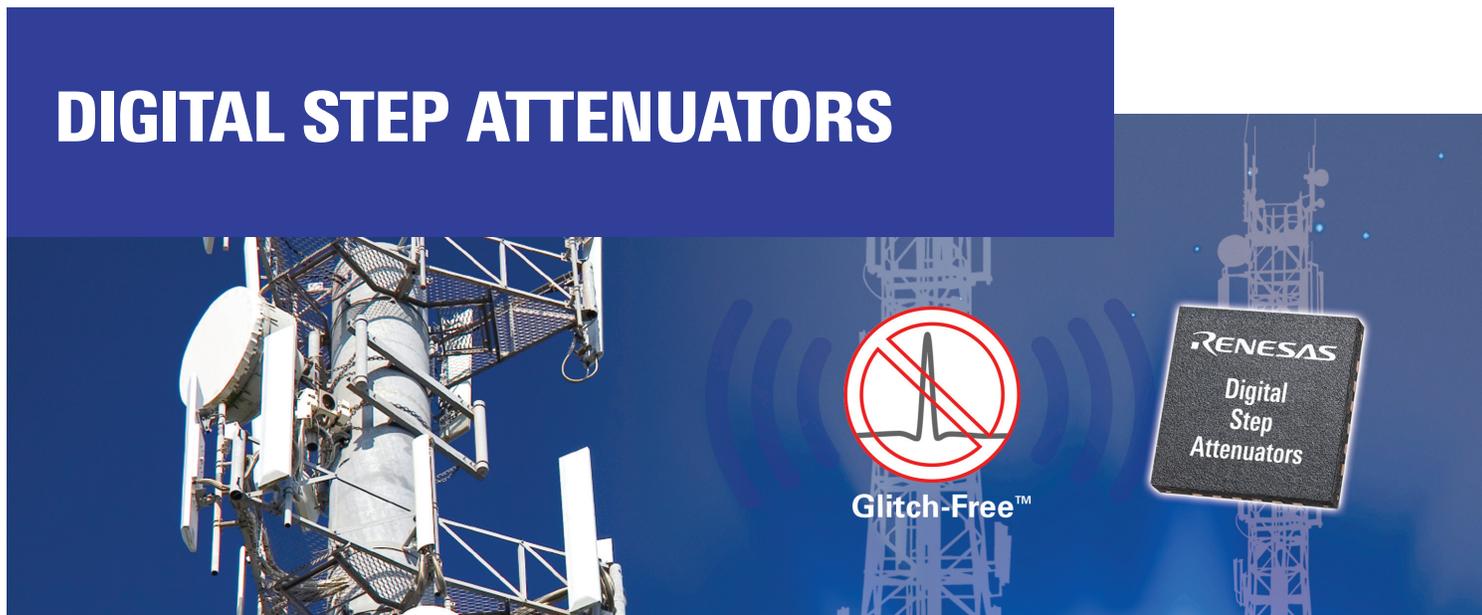


# DIGITAL STEP ATTENUATORS



Renesas Digital Step Attenuators (DSAs) are extremely accurate, enabling precise adjustment of the DSA attenuation value to the desired level with pinpoint accuracy. The step and absolute accuracy hold very well over temperature ( $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ) which helps customers simplify their software interface. The Glitch-Free technology results in a typical settling time of 400 nsec making them ideal for agile TDD systems. These devices are bi-directional with very high power handling characteristics with up to a 28 dBm continuous power rating at  $105^{\circ}\text{C}$  and  $> 34\text{dBm}$  compression point.

Renesas DSAs have a typical insertion loss as low as 1.2dB at 2GHz. Low insertion loss improves overall system performance and data throughput, helping improve receiver sensitivity and minimize unwanted signal loss in the transmitter path.

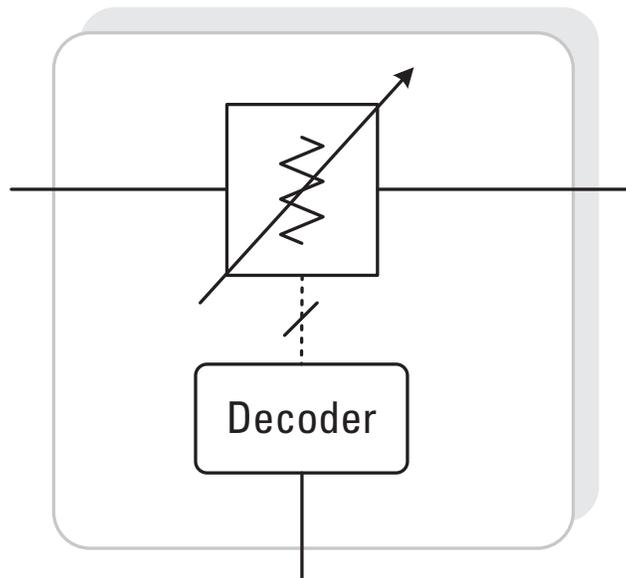
Unwanted signals can generate intermodulation (IM) products, reducing the effective SNR and signal throughput of the system. Applications such as 4G LTE, CATV infrastructure and fiber access networks have stringent linearity requirements in order to achieve high system data rates, driving the need for high linearity RF components that minimize IM3 distortion. Renesas DSAs are very low distortion devices with typical IP3 of only +65 dBm, making them an ideal choice for applications that require high linearity.

## Advantages

- Glitch-Free™ Technology:
  - Reduces transient glitches by up to 95%
  - Results in as little as 0.6 dB of overshoot ringing during MSB transitions
- Step error of  $\sim 0.1\text{dB}$  typical
- Typical absolute attenuation error of  $\pm 0.2\text{ dB}$
- Low insertion loss: typically 1.2 dB @ 2 GHz
- Very low distortion devices: typical IP3 of +65 dBm
- Silicon-based semiconductor technology
- Very high power handling  $>34\text{ dBm}$  compression point
- Supports  $50\Omega$  and  $75\Omega$  impedances

# DIGITAL STEP ATTENUATORS

Part Number	Description	Frequency (GHz)	Max Att. (dB)	Resolution (dB)	IL (dB)	IP0.1dB (dBm)	IIP3 (dBm)	Voltage (V)	Current (mA)	Package (mm)
F1912	6-bit	0.001 – 4	31.5	0.5	1.4	31	60	3.3	0.55	4 x 4, 20-Pin
F1950	7-bit	0.15 – 4	31.75	0.25	1.3	27.5	63	3.3	0.25	4 x 4, 24-Pin
F1951	6-bit	0.1 – 4	31.5	0.5	1.2	29	64	3.3	1.1	4 x 4, 24-Pin
F1953	6-bit	0.4 – 4	31.5	0.5	1.4	28.5	66	3	0.2	4 x 4, 20-Pin
F1956	7-bit	0.001 – 6	31.75	0.25	1.6	34.5	64	3.3	0.35	5 x 5, 32-Pin
F1958	7-bit	0.001 – 6	31.75	0.25	1.6	35	64	3.3	0.25	4 x 4, 24-Pin
F1975	6-bit, 75Ω	0.005 – 3	31.5	0.5	1.2	30.5	64	3.3	0.55	4 x 4, 20-Pin
F1977	7-bit, 75Ω	0.005 – 3	31.75	0.25	1.4	32	64	3.3	0.322	5 x 5, 32-Pin
F1978	6-bit, 75Ω	0.005 – 3	31.5	0.5	1.2	30.5	64	3.3	0.55	4 x 4, 20-Pin



Renesas Digital Step Attenuator block diagram

To request samples, download documentation or learn more visit: [idt.com/rfattenuator](http://idt.com/rfattenuator)



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